WHAT IS CLAIMED IS:

1. A solid-state detector comprising:

a pixilated semiconductor detector having plurality of individual indium bumps arrayed on a surface of the detector, wherein the indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, and the indium bumps have a height of between 15 to about 100μm.

2. The solid-state detector of claim 1 wherein the indium bumps have a height of between 20 to about 70μm.

3. The solid-state detector of claim 1 wherein the pixilated detector is selected from the group consisting of Si, Ge, HgI, CdTe, and CdZnTe semiconductors.

4. A readout chip comprising VLSI chip having a plurality of individual indium bumps arrayed on a surface of the chip, wherein the indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, and the indium bumps have a height ranging from 15 to 100μm.

5. A hybrid detector comprising a pixilated detector in electrical contact with a VLSI chip, wherein the detector and

the VLSI chip each have a surface with regions adapted to forming electrical contacts, and wherein electrical contacts formed from indium metal are made between the pixels of the semiconductor detector and regions on the VLSI chip corresponding thereto, and wherein the surfaces of pixilated detector and the VLSI chip are separated by about 15 to about 100μm.

6. A method of forming predetermined electrical contacts on a detector comprising:

constraining a shadow mask having an array of holes in desired locations 10 to 100μm above a surface on the detector, aligning the mask above the detector, and evaporating indium metal under vacuum through holes in the mask onto the surface of the detector to form the contacts.

7. The method of claim 6, further comprising the step of bump-bonding the detector to readout chip that has indium bumps similarly positioned upon a surface.

8. A method of forming predetermined electrical contacts on a chip comprising:

the steps of constraining a shadow mask having an array of holes in desired locations about 10 to about 100μm above a

surface on the chip, aligning the mask above the chip, and evaporating indium metal under vacuum through holes in the mask onto the surface of the chip to form the contacts.